Concurrent Algorithms Exercise 2 September 30, 2014

Problem 1.

- 1. Devise an algorithm that implements an atomic *M*-valued SWMR register using (any number of) atomic binary SWMR registers.
- 2. Prove that your algorithm is correct.
- 3. Explain whether your algorithm remains correct (i.e., implements an atomic register) if you change the binary base registers from atomic to regular.