The Limitations of Registers (cont'd)

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Is it possible to wait-free implement a consensus object from stacks and registers in a system of 2 processes?

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Validity A decided value is a proposed value.

Two Processes Consensus from a Stack and Registers

initialization
  $REG[0] \leftarrow \bot; REG[1] \leftarrow \bot$
  $S.push(\text{loser}); S.push(\text{winner})$
operation $\textsc{propose}(v)$
  $REG[id] \leftarrow v$
  if $S.pop() = \text{winner}$ **then**
    return v
  else
    return $REG[1 - id]$

The Case of Three Processes

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- Even with several stacks and more registers, how to organize?

Is it possible to wait-free implement a consensus object from stacks and registers in a system of 3 processes?

- Suppose that there exists an algorithm solving 3 processes consensus from stacks and registers.

Structure of the Proof

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- Show that there is a schedule in which a process takes an infinite number of steps but does not decide.

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- Show that there is a schedule in which a process takes an infinite number of steps but does not decide.
- This contradicts the termination property. Consequently, there is no such algorithm.

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- Starting from $C(0,1,0)$, if p_2 executes alone, it has to decide 1 because it cannot distinguish between this execution and the one starting by $C(1,1,1)$ where it executes alone.
- Consequently, $C(0,1,0)$ is bivalent.

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- Let op_i (resp. op_j) be the next step executed by p_i (resp. p_j) in $\Sigma(C(0,1,0))$.
- If op_i and op_j commute, then processes cannot distinguish between $p_i(p_j(\Sigma(C(0,1,0))))$ and $p_j(p_i(\Sigma(C(0,1,0))))$ while one is 0-valent and the other is 1-valent. This is a contradiction.

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- Two reads on the same register commute, so if op_i and op_j are both accesses to the same register, at least one of them is a write.
- If they are both writes to the same register, then p_i cannot distinguish between $p_i(\Sigma(C(0,1,0)))$ and $p_i(p_j(\Sigma(C(0,1,0))))$, while one is 0-valent and the other 1-valent. This is a contradiction.

Possible Values for op_i and op_j

- If op_i is a write to a register and op_j a read to the same register, then p_i cannot distinguish between $p_i(p_j(\Sigma(C(0,1,0))))$ and $p_i(\Sigma(C(0,1,0)))$ while the former is 1-valent and the latter is 0-valent. This is a contradiction.

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- Symmetric arguments apply when inverting the valence of $p_i(\Sigma(C(0,1,0)))$ and $p_j(\Sigma(C(0,1,0)))$ or when op_i and op_j are respectively a read and a write to the same register.

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- It follows that op_i and op_j are necessarily invocations of operations on the same stack.

Possible Values for op_i and op_j

- If both op_i and op_j are pop operations on the same stack, then $p_k, k \in \{1, 2, 3\} \setminus \{i, j\}$ cannot distinguish between $p_i(p_j(\Sigma(C(0, 1, 0))))$ and $p_j(p_i(\Sigma(C(0, 1, 0))))$ while one is 0-valent and the other 1-valent. This is a contradiction.

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- If op_i is a push operation and op_j a pop operation on the same stack, then we have two cases:
  - If in $\Sigma(C(0, 1, 0))$ the stack is empty, then p_k cannot distinguish between $p_j(p_i(\Sigma(C(0, 1, 0))))$ and $p_j(\Sigma(C(0, 1, 0))))$ while the former is 0-valent and the latter is 1-valent. This is a contradiction.

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- If op_i is a push operation and op_j a pop operation on the same stack, then we have two cases:
  - If in $\Sigma(C(0,1,0))$ the stack is empty, then p_k cannot distinguish between $p_j(p_i(\Sigma(C(0,1,0))))$ and $p_j(\Sigma(C(0,1,0))))$ while the former is 0-valent and the latter is 1-valent. This is a contradiction.
  - If in $\Sigma(C(0,1,0))$ the stack is not empty, then we need a further analysis.

Possible Values for op_i and op_j

In this case op_i is a push operation and op_j a pop operation on the same stack that is not empty in $\Sigma(C(0,1,0))$.

- If p_i runs alone from $p_j(p_i(\Sigma(C(0,1,0))))$, it necessarily eventually pops the item z that was on top of the stack in $\Sigma(C(0,1,0))$ or it would not distinguish between the situation when it runs alone from $p_i(p_j(\Sigma(C(0,1,0))))$ while it has to decide 0 in the first situation and 1 in the second.

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- Let Σ_i be the schedule in which p_i executes solo from $p_j(p_i(\Sigma(C(0,1,0))))$ until just after it pops the item z.
- Since until this pop operation p_i cannot distinguish if it started from $p_j(p_i(\Sigma(C(0,1,0))))$ or $p_i(p_j(\Sigma(C(0,1,0))))$, it also takes the same steps while running alone from the later configuration. The only difference is the value it pops at the last step of Σ_i.

- p_k cannot distinguish between $\Sigma_i(p_j(p_i(\Sigma(C(0,1,0)))))$ and $\Sigma_i(p_i(p_j(\Sigma(C(0,1,0)))))$ because the stack is in the same state in both configurations. The former configuration being 0-valent while the latter is 1-valent, this is a contradiction.

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- The same reasoning applies if the roles of p_i and p_j swapped.

Possible Values for op_i and op_j

- If op_i and op_j are both push operations on the same stack, then, when running alone from $p_i(p_j(\Sigma(C(0,1,0))))$, p_i necessarily eventually pops the item it pushed at op_i or it would not be able to distinguish this execution from the one when it runs alone from $p_j(p_i(\Sigma(C(0,1,0))))$.

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- Let Σ'_i be the schedule in which p_i executes alone from $p_i(p_j(\Sigma(C(0,1,0))))$ until just after it pops the value pushed by op_i.
- With the same reasoning, starting from $\Sigma'_i(p_i(p_j(\Sigma(C(0,1,0)))))$ or from $\Sigma'_i(p_j(p_i(\Sigma(C(0,1,0)))))$, p_j necessarily take the same steps until it eventually pops the value pushed by op_j (in the first situation) or by op_i (in the second one). Let us denote Σ'_j its steps until just after this pop.

- p_k is not able to distinguish between $\Sigma'_j(\Sigma'_i(p_i(p_j(\Sigma(C(0,1,0))))))$ and $\Sigma'_j(\Sigma'_i(p_j(p_i(\Sigma(C(0,1,0))))))$. This is a contradiction because the former is 1-valent while the latter is 0-valent.

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- In all cases we reach a contradiction. It follows that there exists a schedule such that a process takes an infinite number of steps without deciding, which concludes the proof.

It is impossible to wait-free implement consensus among 3 processes from stacks and registers.

Immediate Snapshot Specification

An immediate snapshot object offers an operation WRITE-SNAPSHOT(v) that can be invoked at most once by each process. It returns a set *view* of pairs (j, v_j) where j is a process identifier and v_j a value. If we denote by $view_i$ the set returned to process i, we have the following properties:

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Containment $\forall i, j \ : \ view_i \subseteq view_j \vee view_j \subseteq view_i$.

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Immediacy $\forall i, j \ : \ (j, v_j) \in view_i \implies view_j \subseteq view_i$.

Theorem

$$((i, v_i) \in view_j \wedge (j, v_j) \in view_i) \implies view_i = view_j$$

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Consequence

The calls to an immediate snapshot object can be set-linearized by ordering the processes according to the size of their views.

One by one:
$view_1 = \{(1, v_1)\} \subsetneq view_2 = \{(1, v_1), (2, v_2)\} \subsetneq view_3 = \{(1, v_1), (2, v_2), (3, v_3)\}$

Two then one:
$view_1 = view_2 = \{(1, v_1), (2, v_2)\} \subsetneq view_3 = \{(1, v_1), (2, v_2), (3, v_3)\}$

Three together:
$view_1 = view_2 = view_3 = \{(1, v_1), (2, v_2), (3, v_3)\}$

Immediate Snapshot Algorithm

initialization
$\quad REG[1,\ldots,n][1,\ldots,n] \leftarrow [[\perp,\ldots,\perp],\ldots,[\perp,\ldots,\perp]]$
operation $\textsc{write-snapshot}(v)$
$\quad$ return $\textsc{rec\_write-snapshot}(n, v)$
operation $\textsc{rec\_write-snapshot}$(x,v)
$\quad REG[x][id] \leftarrow v$
$\quad$ **for** $j \in \{1,\ldots,n\}$ **do** $scan[j] \leftarrow REG[x][j]$ **end for**
$\quad view \leftarrow \{(j, scan[j]) \mid scan[j] \neq \perp\}$
$\quad$ **if** $|view| = x$ **then**
$\quad\quad$ return *view*
$\quad$ **else**
$\quad\quad$ return $\textsc{rec\_write-snapshot}(x-1, v)$

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- It then updates its state to include the knowledge it has gained on the state of other processes and proceeds to the next round.
- After a predetermined number of rounds R, a process that does not crash decides a value by applying a deterministic function DECIDE of its final state.

The Iterated Immediate Snapshot Model

initialization

  $s \leftarrow \{\langle 0, \text{input of the process} \rangle\}$

  $r \leftarrow 1$

while $r \leq R$ **do**

  $view \leftarrow IS[r].\text{WRITE-SNAPSHOT}(s)$

  $s \leftarrow s \cup \{\langle r, view \rangle\}$

  $r \leftarrow r + 1$

$\text{DECIDE}(s)$

The Read/Write Wait-free Model vs. $\mathcal{IIS}$

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A one-shot colorless task can be solved in the read/write wait-free model iff it can be solved in $\mathcal{IIS}$.

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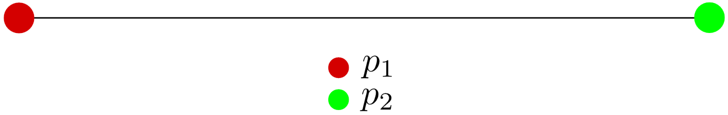
- The possible executions of an algorithm in $\mathcal{IIS}$ between two processes can be seen as a subdivision of the initial configuration.



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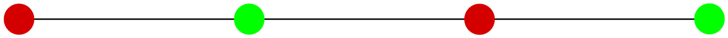

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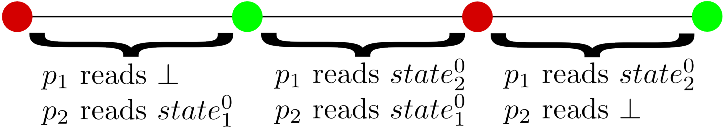

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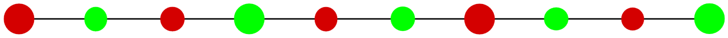

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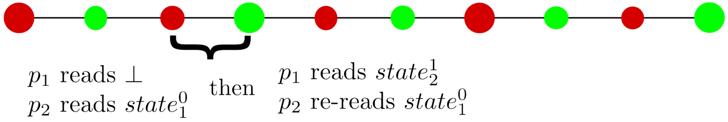
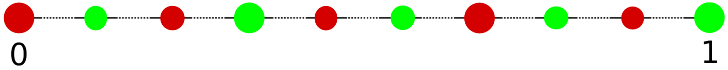


Solving Consensus is impossible in $\mathcal{IIS}$ with Two Processes

- The possible executions of an algorithm in $\mathcal{IIS}$ between two processes can be seen as a subdivision of the initial configuration.
- The processes have to decide in a finite number of rounds R, the subdivision is consequently finite.



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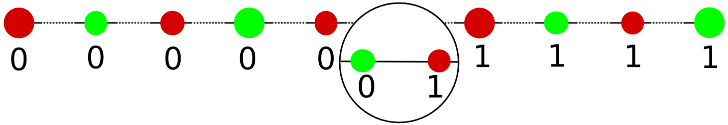

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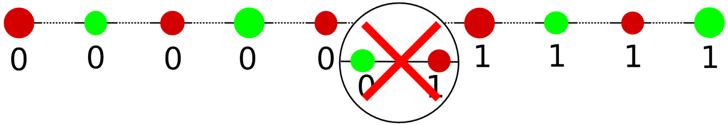
- Impossibility result comes from Sperner's Lemma.



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2-Set Agreement from Registers Among 3 Processes

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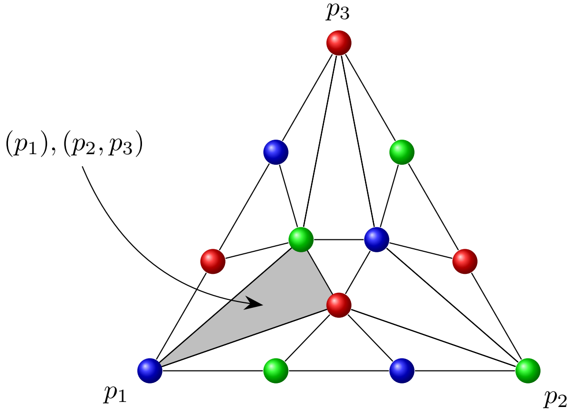
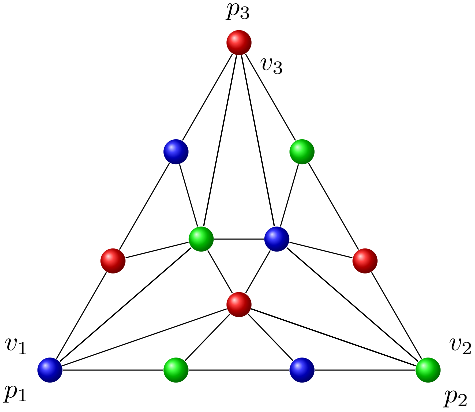


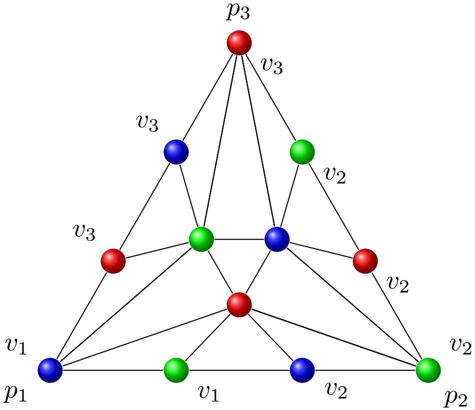
2-Set Agreement from Registers Among 3 Processes

If a process runs alone, it has to decide its input.



2-Set Agreement from Registers Among 3 Processes

If two processes run without seeing the third one, they have to decide on one of their two values.



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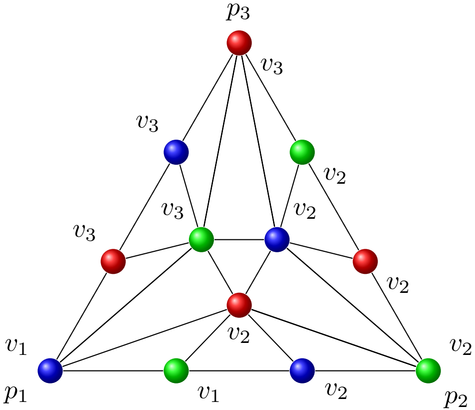

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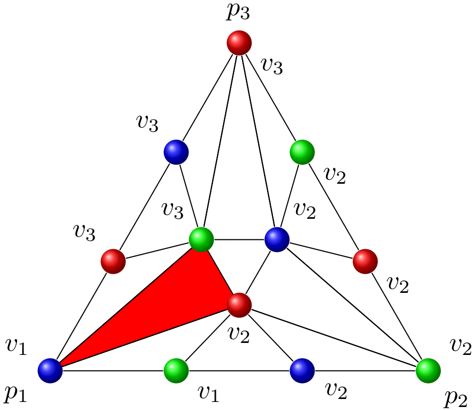
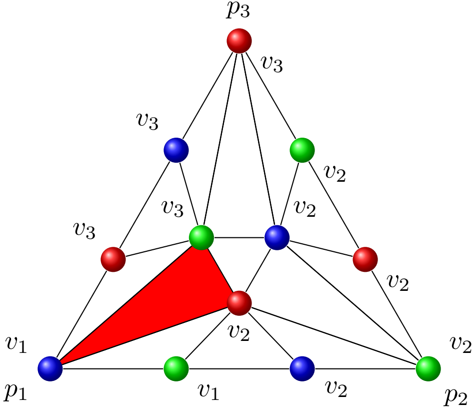
has at least one configuration where processes decide on 3 different values.



2-Set Agreement from Registers Among 3 Processes

2-set agreement is consequently impossible in one round of $\mathcal{IIS}$ between 3 processes, but the same argument applies for any finite number R of rounds.



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- It follows that k-set agreement cannot be wait-free implemented from registers in a system of $k + 1$ processes.

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- Combining the two results, we show that k-set agreement is impossible from registers in a system prone to k crashes or more.

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