The Limitations of Registers

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Registers

• **Question 1:** what objects can we implement with registers? *Counters* and *snapshots* (previous lecture)

• **Question 2:** what objects we cannot implement? (this lecture)
Shared memory model

Registers

P1

P2

P3
Shared memory model

Counters

Registers

Snapshots

P1

P2

P3
Shared memory model

Counters
Snapshots
Queue?

Registers

Fetch&Inc?
Fetch&Inc

- A counter that contains an integer

- Operation fetch&inc() increments the counter and returns the new value
The consensus object

- One operation `propose()` which returns a value. When a propose operation returns, we say that the process decides.

- No two processes decide differently.

- Every decided value is a proposed value.
The consensus object

- **Proposition:**
  - *Consensus* can be implemented among two processes with *Fetch&Inc* and *registers*.

- Proof (algorithm): consider two processes $p_0$ and $p_1$ and two *registers* $R_0$ and $R_1$ and a *Fetch&Inc* $C$. 
2-Consensus with Fetch&Inc

- Uses two registers R0 and R1, and a Fetch&Inc object C (with one fetch&inc() operation that returns its value)
- (NB. The value in C is initialized to 0)

- Process pl:

  - propose(vI)
  - R{1-I}.write(vI)
  - val := C.fetch&inc()
  - if(val = 1) then
    return(vI)
  - else return(R{1-I}.read())
Proposition: No asynchronous deterministic algorithm implements consensus among two processes using only registers

Corollary: No algorithm implements Fetch&Inc among two processes using only registers
Queue

- The queue is an object container with two operations: \textit{enq()} and \textit{deq()}

- Can we implement a (atomic wait-free) \textit{queue}?
2-Consensus with queues

Uses two registers R0 and R1, and a queue Q
Q is initialized to \{winner, loser\}

Process pI:

```
propose(vI)
   R1.write(vI)
   item := Q.dequeue()
   if item = winner return(vI)
   return(R{1-l}.read())
```
\[ W(0) \quad \text{Deq() -> winner} \quad \text{Return(0)} \]

\[ W(1) \quad \text{Deq() -> loser} \quad \text{Return(0)} \]
Correctness

Proof (algorithm):

- (wait-freedom) by the assumption of a wait-free register and a wait-free queue plus the fact that the algorithm does not contain any wait statement
- (validity) If \( p_I \) dequeues winner, it decides on its own proposed value. If \( p_I \) dequeues loser, then the other process \( p_J \) dequeued winner before. By the algorithm, \( p_J \) has previously written its input value in \( R_J \). Thus, \( p_I \) decides on \( p_J \)'s proposed value;
- (agreement) if the two processes decide, they decide on the value written in the same register.
More consensus implementations

- A **Test&Set** object maintains binary values $x$, init to 0, and $y$; it provides one operation: \texttt{test&set()}
  - Sequential spec:
    - test&set() \{ $y := x; x := 1; \text{return}(y);$ \}

- A **Compare&Swap** object maintains a value $x$, init to $\bot$, and provides one operation: \texttt{compare&swap(v,w)};
  - Sequential spec:
    - \texttt{c&s(old,new) \{ if x = old then x := new; \text{return}(x)\}}
2-Consensus with Test&Set

- Uses two registers R0 and R1, and a Test&Set object T

- Process pI:

  propose(vI)
  RI.write(vI)
  val := T.test&set()
  if(val = 0) then
    return(vI)
  else return(R{1-I}.read())
N-Consensus with C&S

- Uses a C&S object C

- Process pl:
  - propose(vl)
  - val := C.c&s(⊥,vl)
  - if(val = ⊥) then
    - return(vl)
    - else return(val)
Impossibility [FLP85,LA87]

- **Proposition:** No asynchronous deterministic algorithm implements **consensus** among two processes using only **registers**

- **Corollary:** No algorithm implements a **queue** (*Fetch&Inc,...*) among two processes using only **registers**
Registers

- **Question 1**: what objects can we implement with registers? *Counters* and *snapshots* (previous lecture)

- **Question 2**: what objects we cannot implement? All objects that (together with *registers*) can implement *consensus* (this lecture)
Proposition: no algorithm implements consensus among two processes using only registers

Proof (by contradiction): consider two processes p0 and p1 and any number of registers, R1..Rk..
Assume that a consensus algorithm A for p0 and p1 exists.
Elements of the model

- A **configuration** is a global state of the distributed system

- A new configuration is obtained by executing a **step** on a previous configuration: the step is the unit of execution
Elements of the model

- The adversary decides which process executes the next step and the algorithm deterministically decides the next configuration based on the current one
Distributed computing is a game
A game between an adversary and a set of processes
The adversary decides which process goes next

The processes take steps
Elements of the model

- The adversary decides which process executes the next step and the algorithm deterministically decides the next configuration based on the current one
Elements of the model

- **Schedule**: a sequence of steps represented by process ids
- The schedule is chosen by the system
- An asynchronous system is one with no constraint on the schedules: any sequence of process ids is a schedule
Consensus

- The algorithm must ensure that *agreement* and *validity* are satisfied in every schedule

- Every process that executes an infinite number of steps eventually decides
Impossibility (elements)

- (1) a (initial) **configuration** $C$ is a set of (initial) values of $p_0$ and $p_1$ together with the values of the registers: $R_1..R_k,..$;
- (2) a **step** is an elementary action executed by some process $p_i$: it consists in reading or writing a value in a register and changing $p_i$’s state according to the algorithm $A$;
- (3) a **schedule** $S$ is a sequence of steps; $S(C)$ denotes the configuration that results from applying $S$ to $C$. 
Impossibility (elements)

- Consider $u$ to be 0 or 1; a configuration $C$ is $u$-valent if, starting from $C$, no matter how the processes behave, no decision other than $u$ is possible.

- We say that the configuration is univalent. Otherwise, the configuration is called bivalent.
P0(0)  \[ \begin{array}{c} \text{W}(X) \\ \text{RI} \end{array} \quad \begin{array}{c} \text{R}() -> \text{Y} \\ \text{RJ} \end{array} \quad \text{Return}(0) \]

P1(0)  \[ \begin{array}{c} \text{W}(Z) \\ \text{RK} \end{array} \quad \begin{array}{c} \text{W}(V) \\ \text{RL} \end{array} \quad \text{Return}(0) \]
\[ P0(1) \quad W(X) \quad R() \rightarrow Y \quad \text{Return}(1) \]

\[ P1(1) \quad W(Z) \quad W(V) \quad \text{Return}(1) \]
P0(1) \[\begin{array}{c} W(X) \\ RI \\ \end{array} \quad \begin{array}{c} R() \rightarrow Y \\ RJ \\ \end{array} \quad \text{Return}(1/0) \]

P1(0) \[\begin{array}{c} W(Z) \\ RK \\ \end{array} \quad \begin{array}{c} W(V) \\ RL \\ \end{array} \quad \text{Return}(1/0) \]
Impossibility (structure)

- **Lemma 1:** there is at least one initial *bivalent* configuration

- **Lemma 2:** given any bivalent configuration C, there is an *arbitrarily long schedule* S(C) that leads to another bivalent configuration
The conclusion

- Lemmas 1 and 2 imply that there is a configuration C and an *infinite* schedule S such that, for any prefix S’ of S, S’(C) is bivalent.

- In infinite schedule S, at least one process executes an infinite number of steps and does not decide

- A contradiction with the assumption that A implements consensus.
Lemma 1

The initial configuration $C(0,1)$ is bivalent

Proof: consider $C(0,0)$ and $p_1$ not taking any step: $p_0$ decides 0; $p_0$ cannot distinguish $C(0,0)$ from $C(0,1)$ and can hence decides 0 starting from $C(0,1)$; similarly, if we consider $C(1,1)$ and $p_0$ not taking any step, $p_1$ eventually decides 1; $p_1$ cannot distinguish $C(1,1)$ from $C(0,1)$ and can hence decides 1 starting from $C(0,1)$. Hence the bivalency.
Lemma 2

Given any bivalent configuration $C$, there is an arbitrarily long schedule $S$ such that $S(C)$ is bivalent

Proof (by contradiction): let $S$ be the schedule with the maximal length such as $D = S(C)$ is bivalent; $p_0(D)$ and $p_1(D)$ are both univalent: one of them is 0-valent (say $p_0(D)$) and the other is 1-valent (say $p_1(D)$)
Lemma 2

- Proof (cont’d): To go from D to p0(D) (vs p1(D))
  p0 (vs p1) accesses a register; the register must be the same in both cases; otherwise p1(p0(D)) is the same as p0(p1(D)): in contradiction with the very fact that p0(D) is 0-valent whereas p1(D) is 1-valent
Lemma 2

Proof (cont’d): To go from D to p0(D), p0 cannot read R; otherwise R has the same state in D and in p0(D); in this case, the registers and p1 have the same state in p1(p0(D)) and p1(D); if p1 is the only one executing steps, then p1 eventually decides 1 in both cases: a contradiction with the fact that p0(D) is 0-valent; the same argument applies to show that p1 cannot read R to go from D to p1(D).

Thus both p0 and p1 write in R to go from D to p0(D) (resp., p1(D)). But then p0(p1(D))= p0(D) (resp. p1(p0(D))= p1(D)) --- a contradiction.
The conclusion (bis)

Lemmas 1 and 2 imply that there is a configuration C and an *infinite* schedule S such that, for any prefix S’ of S, S’(C) is bivalent.

In infinite schedule S, at least one process executes an infinite number of steps and does not decide.

A contradiction with the assumption that A implements consensus.